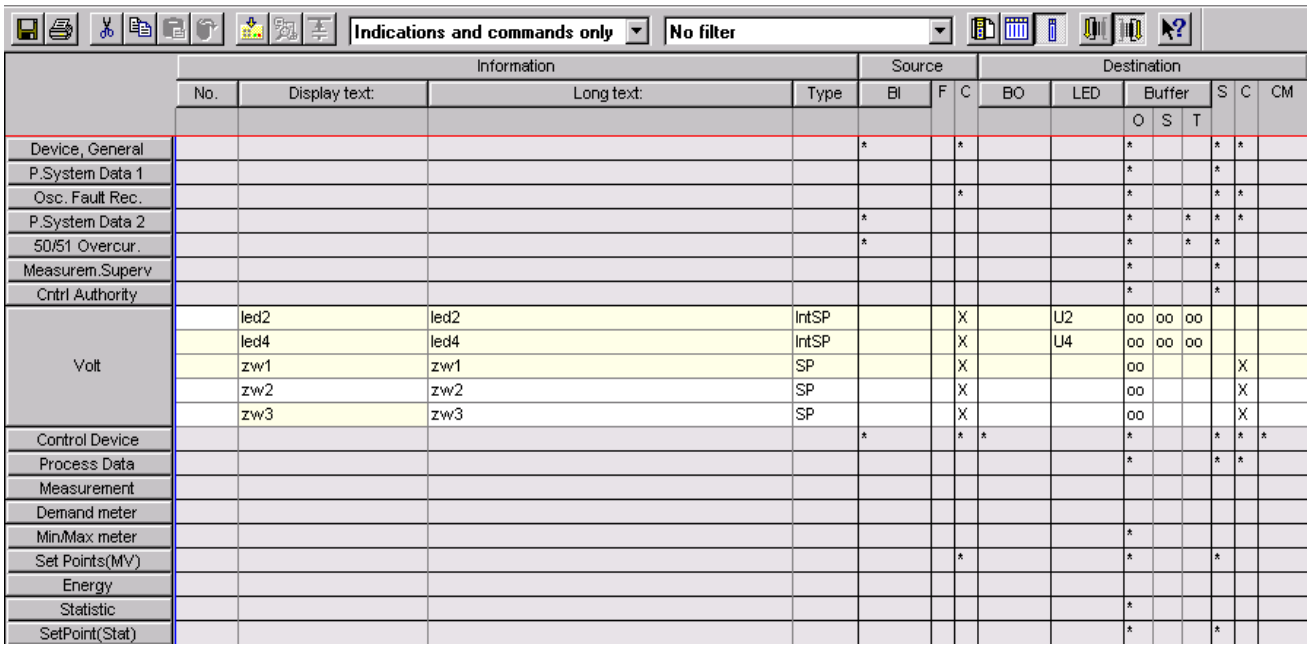
Different speeds of voltage drop

A logic to distinguish between rapid and slow voltage decrease can be implemented in the device.

In this example, two conditions will be detected. The first condition will be detected by the protection device as a slow voltage drop. This state arises when the voltage decrease from 95 to 85% of rated voltage takes longer than 5 to 10 seconds. In this event, an output signal for load-shedding must be operated. In case the voltage drops instantaneously, i.e. from 100% to below 85% of rated voltage within a 1 second window, the load-shedding output must be inhibited and a signal indicating this state may be released.

For this application measured values must be routed to the CFC logic. Two CFC charts are required, when one-phase voltage is monitored as in this case.



	Information				Source			Destination							
	No.	Display text:	Long text:	Type	BI	F	C	BO	LED	Buffer			S	C	CM
										O	S	T			
Device, General					*		*			*			*	*	
P.System Data 1										*			*		
Osc. Fault Rec.							*			*			*	*	
P.System Data 2					*					*		*	*	*	
50/51 Overcur.					*					*		*	*		
Measurem.Superv										*			*		
Cntrl Authority										*			*		
Volt		led2	led2	IntSP			X		U2	oo	oo	oo			
		led4	led4	IntSP			X		U4	oo	oo	oo			
		zw1	zw1	SP			X			oo				X	
		zw2	zw2	SP			X			oo				X	
		zw3	zw3	SP			X			oo				X	
Control Device					*		*	*		*			*	*	*
Process Data										*			*	*	
Measurement															
Demand meter															
Min/Max meter										*					
Set Points(MV)							*			*			*		
Energy															
Statistic										*					
SetPoint(Stat)										*			*		

Picture 1 : input-output matrix with new user-defined annunciations

First new annunciations must be applied in the input/output matrix.
For the sake of clarity it is better to create a new group in the input/output matrix (in this case *Volt*.)

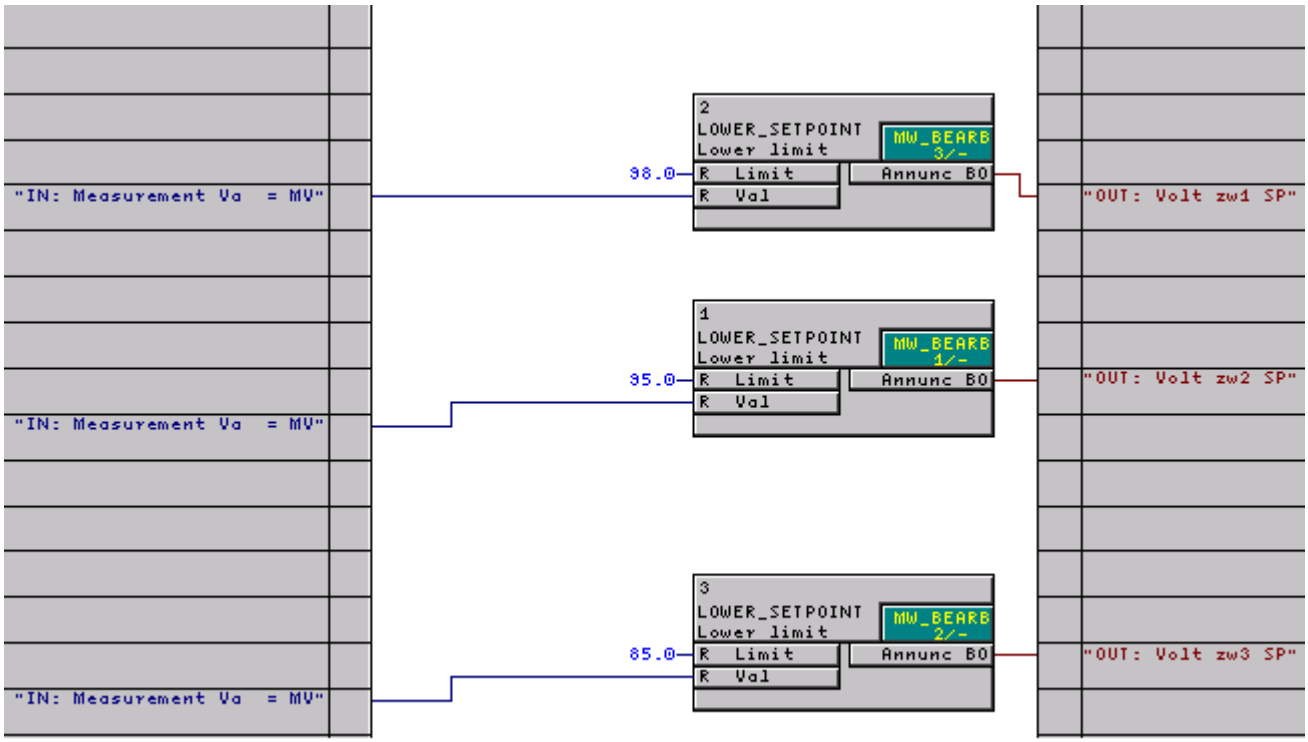
Five new annunciations are assigned to this group. The first two are internal single point annunciations. Their source is the CFC chart and they are routed to the LEDs for visual indication.

The Led 4 indicates that the logic has ultimately timed out. The other three signals (zw1, zw2, zw3) are single point information type. Their source and destination are CFC as they are used to connect the CFC charts together. (see picture 1)

The next step is to create the CFC charts. In the first chart three lower set-point gates are applied. The Val inputs of all three gates are routed to the Va phase voltage. This phase voltage is available in the CFC chart (measurement values execution layer) because its destination in the I/O matrix was the CFC chart – default setting of the device.

Three thresholds are used in this task - 100%, 95% and 85%. The logic detects whether the A-phase voltage is below any one of these three levels. The output signal of the lower set point gates are routed to the zw1, zw2 and zw3 single point annunciations. (see picture 2).

These signals are used as inputs to the next CFC chart:
-Lower set point detecting if voltage is below 100 % corresponds to *zw1* annunciation
-Lower set point detecting if voltage is below 95 % corresponds to *zw2* annunciation
-Lower set point detecting if voltage is below 85 % corresponds to *zw3* annunciation



Picture 2 : CFC chart with measurement thresholds

Next, the information from the measurement chart must be applied to the logic chart. The sequence of the gates must be in the correct order. The lower set point gates will be in the measurement layer, the other logic gates must be in the slow PLC layer. Timer gates do not function in the measurement layer.

The zw1, zw2 and zw3 signals are evaluated to determine if any one of them is picked upped to indicate a voltage drop condition.

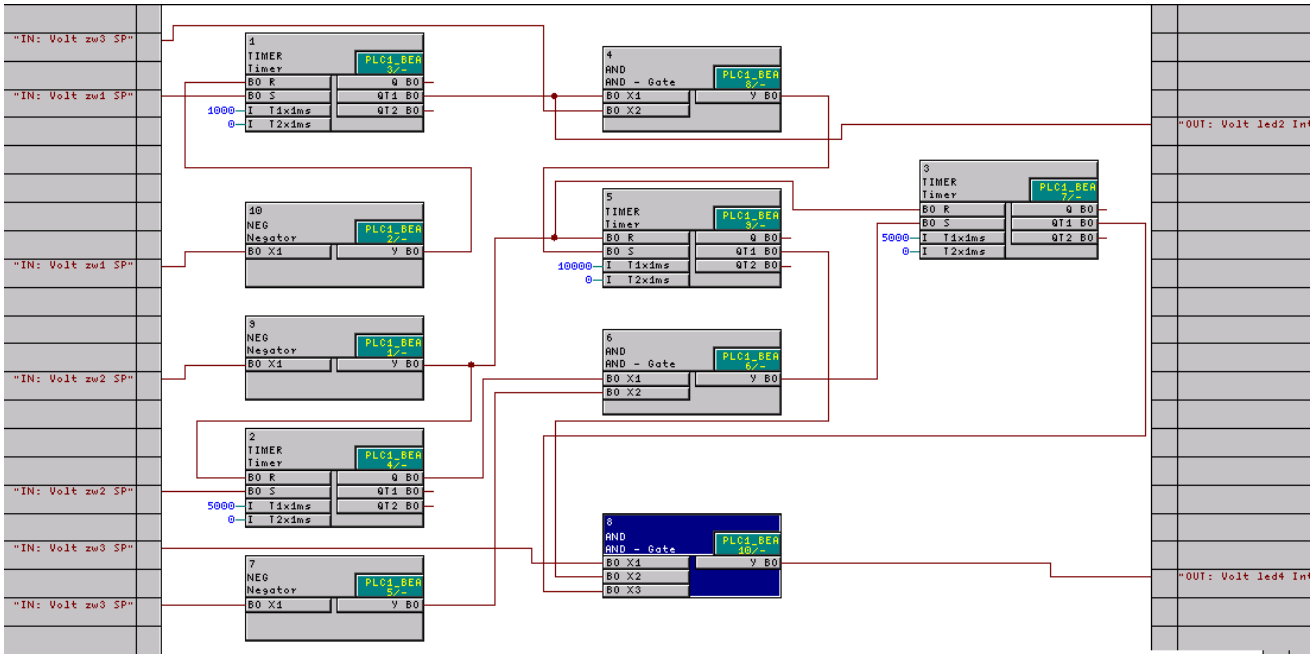
The input signal for timer 2 is zw2 (95%) information from first CFC chart. If this condition persists for longer than 5 seconds, the Q output of timer 2 issues a logic 1. This is connected to the input of AND gate 6. The other input to AND gate 6 is connected to the negated zw3 (85 %) signal. The output of AND gate 6 will therefor only generate a logic 1 if the voltage drops below 95% but not below 85% for a period of 5 seconds or longer. This condition in turn is then routed to the input of timer 3.

On timer 3 the QT1 output is used which provides a 5 second pulse, which is connected to AND gate 8. A further input of AND gate 8 (BO X1) is the zw3 signal (85%) indicating a voltage below 85%. As long as 85% is not reached in maximum 10 seconds, the output signal for the CB will appear.

The third input to AND gate 8 (BO X2) is a blocking signal which arises when the voltage drops very quickly. The timer 1 input S is the zw1(100%) signal, detecting if the voltage is below the 100% level. This condition causes a 1 second pulse output. This is connected to an input of AND gate 4. A further input of the AND gate 4 is connected to the zw3 signal (85%). If the voltage drops below 100% level and in the same second also drops below 85% of rated voltage, then this will be seen as an instantaneous voltage drop.

If this happens the output signal must be blocked. Therefor AND gate 4 output starts timer 5. This timer 5 QT1 output is connected to AND gate 8 input (BO X2) providing the blocking condition for 10 seconds. The re-set input of timer 5 is provided by the negated zw2 (95 %) signal.

Thereby the timer will be re-set as soon as the voltage rises above 95% . The same is valid for timer 2. (see picture 3).



Picture 3 : CFC chart 2